EECS 312 Final Project:

8-Bit Dual-Mode Ripple-Carry Adder and Accumulator

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April 26, 2026

Contents

1 Team Contributions

The project tasks were distributed to leverage individual strengths while ensuring full system integration through collaborative verification:

- **Soren Walther:** Responsible for the 8-bit ripple-carry adder architecture for transistor sizing optimizations required to meet the 1.56 GHz frequency target.
- **Shashwat Jaguri:** Developed the control MUX logic and performed the fine-tuning/optimization of the register timings. Conducted all power measurement simulations and led the debugging of the testbench to ensure accurate timing analysis.
- **Joshua Lee:** Led the technical report composition and the initial design of the master-slave registers. Developed the primary functional testbench used for adder and accumulation mode verification.
- **Collaboration:** All team members participated in the iterative refinement of the final report and the cross-verification of simulation results.

2 Introduction

This report details the design and verification of an 8-bit dual-mode accumulator and adder system operating at 1.56 GHz in a 1.2V CMOS process. The design optimizes high-speed sequential throughput and power-delay product (PDP) by utilizing a Mirror Adder topology and transmission-gate-based master-slave registers.

3 Design Selection and Justification

3.1 High-Speed Inverter and MUX Design

To maintain signal integrity at 1.56 GHz, "strong" inverters were implemented for critical path nodes, utilizing a 3x increase over baseline minimum-sized devices. The CTRL and RESET logic utilizes 6-transistor transmission-gate multiplexers (four transistors for the gates and two for the select signal inverter), as shown in Figure 1. This configuration minimizes input capacitance and eliminates the V_{th} drop characteristic of standard pass-transistor logic.

3.2 High-Speed Register Implementation

Sequential storage is handled by master-slave transmission-gate registers (Figure 2). While the team initially prototyped a True Single-Phase Clock (TSPC) register to minimize clock distribution overhead, we transitioned to a **transmission-gate-based master-slave architecture** for the final implementation due to:

- **High-Frequency Robustness:** TSPC registers exhibit high sensitivity to clock glitches and require precise transistor sizing to mitigate charge sharing, which poses risks at gigahertz frequencies.
- **Timing Reliability:** The master-slave design provides more predictable setup times and internal propagation delays, ensuring the ripple-carry output is captured only after the logic has settled.
- **Signal Integrity:** By using transmission gates, the design achieves full rail-to-rail swings at internal storage nodes, providing superior noise margins compared to pass-transistor alternatives.

Internal nodes were upsized to ensure the registers meet the 1.56 GHz timing requirements. Optimized sizing details are provided in the Appendix.

3.3 Mirror Adder Logic Selection

The design process initially explored a 28-transistor dynamic adder to lower effective load capacitances. However, this approach was abandoned due to timing mismatches and sizing instabilities encountered during integration into the 8-bit chain. Furthermore, the sensitivity of dynamic nodes to parasitic charge sharing compromised signal integrity at the 1.56 GHz target.

Consequently, a 24-transistor Mirror Adder architecture was selected. This topology is optimized for carry-propagation efficiency. The Mirror Adder produces an inverted carry-out ($\overline{C_o}$) and inverted sum ($\overline{S}$), which reduces the number of serial transistors in the critical path. By prioritizing the carry-propagation chain and applying targeted transistor sizing, we achieved robust switching speeds necessary for 1.56 GHz operation.

3.4 8-Bit Adder Chain Architecture

The 8-bit ripple-carry chain is constructed by cascading eight Mirror Adder stages. The inputs consist of the registered $A\langle 7:0\rangle$ bus and the multiplexed result (Figure 4). The critical path is defined by the sequential carry ripple from the LSB to the final MSB storage registers.

Performance is enhanced by the direct chaining of Mirror Adder modules. Utilizing the inherent inverting property of the Mirror Adder, the $\overline{C_o}$ of one stage is connected directly to the C_i of the subsequent stage. Because the Mirror Adder naturally computes the carry function with inverted logic, this eliminates the need for intermediate inverters between stages, significantly reducing the critical path delay.

4 Circuit Techniques for Optimization

4.1 Gate Sizing and Delay Minimization

To balance low-to-high and high-to-low propagation delays, CMOS components were sized with a 2:1 PMOS-to-NMOS width ratio.

The adder was sized to minimize the critical path, while non-critical components (such as inputs $A[7:1]$ and $B[7:1]$ and sum bits $S[5:0]$) were kept closer to minimum size to reduce power consumption. Inverters were placed strategically at every other bit of S to maintain logical consistency.

Logical effort was applied to approximate the optimal sizing for each component. Initial characterization identified a parasitic capacitance of 0.65 fF/μm for the NMOS devices. Baseline sizing targeted a Fan-out-of-4 (FO4) for components driving heavy loads.

While initial aggressive sizing allowed for speeds near 2 GHz, it resulted in excessive power consumption and significant ripple-through noise. Through iterative simulation and waveform analysis, sizing was refined to preserve functionality and meet frequency targets while optimizing the Power-Delay Product (PDP).

4.2 Zero-Injection Reset Strategy

To preserve the timing margin, we avoided placing a dedicated reset multiplexer within the Sum Register (SREG) feedback loop. Adding logic at this stage would introduce additional gate delay into the critical path. Instead, a "zero-injection" strategy is used: logic `0` values are passed through the A and B register inputs and held for one clock cycle. This effectively clears the system state using the existing datapath, avoiding the hardware overhead and propagation penalties of a dedicated reset network.

4.3 Transistor Width Summary

Per project requirements, only minimum length transistors ($L_{min} = 60$nm) were utilized. The total design width reflects the area required to achieve stable operation within the 640 ps clock period.

Table 1: Cumulative Device Widths (1.56 GHz Design)

Component	**Total NMOS Width (μm)**	**Total PMOS Width (μm)**
8-bit Mirror Adder	58.5	117
8-bit Master-Slave Register	5.76	11.52
Control MUX Logic	8.64	17.28
Total Design Width	**48.96 μm**	**109.44 μm**
Final Total Width	**218.7 μm**	

5 Verification and Methodology

5.1 Critical Path and Propagation Delay Analysis

The critical path for the 8-bit ripple-carry architecture was identified using input patterns that trigger the maximum number of serial gate transitions. In the Mirror Adder, the carry-generation logic is the primary bottleneck; therefore, a signal cascade across all eight stages represents the worst-case delay.

To determine propagation delays ($t_{p,LH}$ and $t_{p,HL}$), we measured the interval from the 50% V_{DD} point of the input transition to the 50% V_{DD} point of the final sum output registers (S_{FF}).

- **High-to-Low Transition ($t_{p,HL}$):** Inputs were set to $01_{16} + FF_{16} \rightarrow 00_{16}$. This forces a carry propagation from LSB to MSB, toggling the final output bit low.
- **Low-to-High Transition ($t_{p,LH}$):** Inputs were set to $01_{16} + 7F_{16} \rightarrow 80_{16}$. This drives the MSB output high through the full carry ripple.

As shown in Figure 5, the highlighted path traces the signal from the LSB transition to the final MSB settling. These measurements confirm that the carry ripple settles within the 640 ps clock period without setup time violations.

Table 2: Propagation Delay Test Patterns

Metric	**Test Pattern**
Worst-Case $t_{p,LH}$	$01_{16} + 7F_{16} = 80_{16}$
Worst-Case $t_{p,HL}$	$01_{16} + FF_{16} = 00_{16}$

5.2 Power Measurement Methodology

Average power consumption (P_{avg}) was measured at the global $V_{DD} = 1.2$V supply node. Power was calculated using the Virtuoso ADE Maestro `integ()` function, integrating the instantaneous product ($V_{DD} \cdot I(t)$) over a steady-state interval.

To ensure data integrity, power was measured over a specific window excluding the initial RESET phase and startup transients. The analysis focused on an eight-cycle window where the system reached a stable switching state.

6 Evaluation and Results

6.1 Frequency-Dependent Power Performance

Power scales linearly with frequency, confirming the dominance of dynamic switching power in the design.

Table 3: Power Performance Summary ($V_{DD} = 1.2$V)

Clock Frequency	**Clock Period (T)**	**Measured Power**	**PDP ($P \times T$)**
500 MHz	2000 ps	136 μW	272 fJ
1 GHz	1000 ps	271 μW	271 fJ
1.5 GHz	666.7 ps	405 μW	270 fJ
Max: 1.56 GHz	**640 ps**	**420 μW**	**268 fJ**

6.2 Functionality and Speed Validation

The 8-bit dual-mode system remained fully functional across all test vectors up to 1.56 GHz. As demonstrated in Table 4, the design operates within a 640 ps clock period, ensuring that storage register (SREG) inputs meet setup requirements.

The 640 ps window represents the operational boundary; beyond 1.56 GHz, the carry ripple fails to reach the MSB bit-slice within the allotted time. Figure 6 documents the transient response, confirming full 1.2V rail-to-rail swings and functional correctness at peak throughput.

7 Conclusion and Summary

This project successfully implemented and verified an 8-bit dual-mode ripple-carry adder and accumulator operating within a 1.2V CMOS process. By leveraging a 24-transistor Mirror Adder architecture and transmission-gate-based master-slave registers, the design optimizes carry-propagation efficiency. Strategic gate sizing and a zero-injection reset strategy minimized the critical path delay, enabling a maximum operational clock frequency of 1.56 GHz (640 ps period) without setup time violations. Furthermore, the system demonstrated efficient, linear frequency-dependent power scaling, consuming 420 µW at peak frequency while maintaining a competitive power-delay product (PDP) of 268 fJ. Ultimately, the finalized architecture successfully balances high-speed sequential throughput, noise margin integrity, and overall power efficiency.

8 References

1. J. M. Rabaey, A. Chandrakasan, and B. Nikolić, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, NJ: Prentice Hall, 2003.

2. S. Akhter, S. Chaturvedi, S. Khan, and A. Bhardwaj, "An Efficient CMOS Dynamic Logic-Based Full Adder," *2020 6th ICSC*, 2020, pp. 226-229.

9 Appendix

9.1 Schematics and Architectural Diagrams

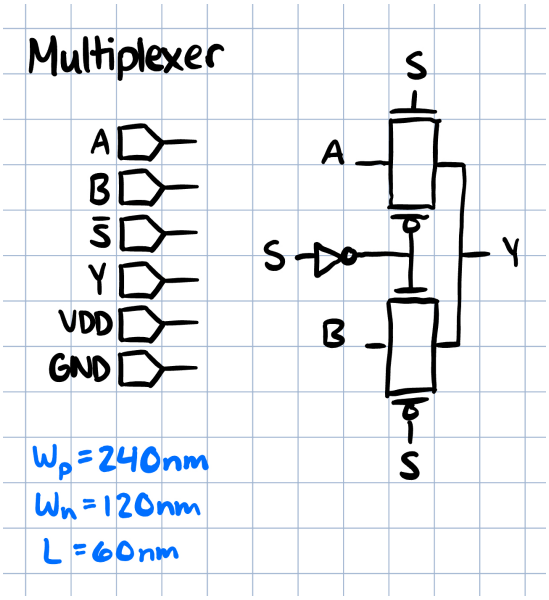

Figure 1: Transistor-level schematic of the 6-transistor transmission-gate MUX.

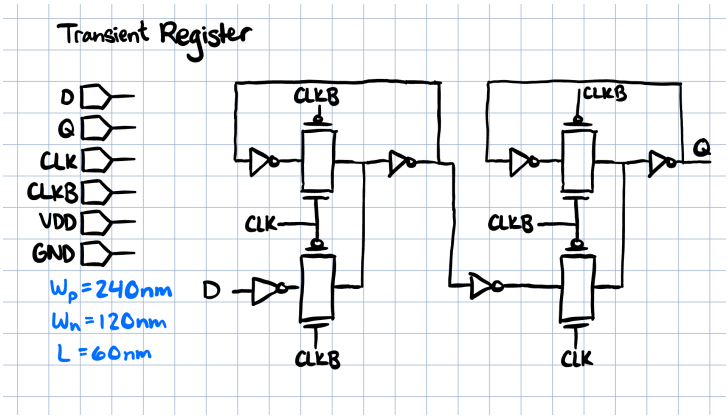

Figure 2: Transistor-level schematic of the master-slave register (utilizing complementary clocks CLK and $CLKB$).

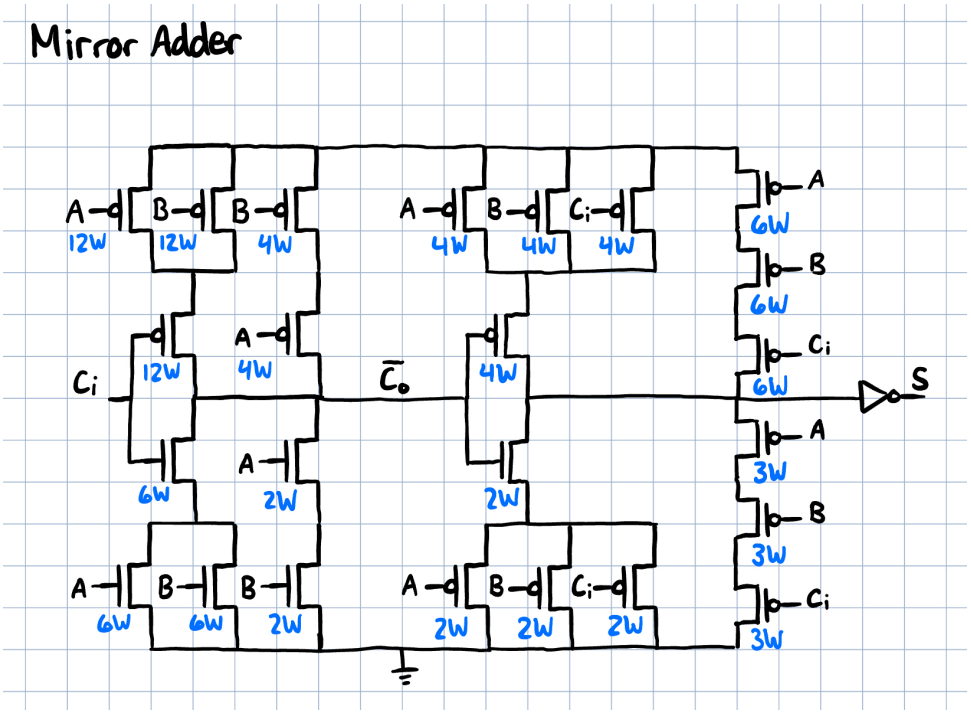

Figure 3: Transistor-level schematic of the 24-transistor Mirror Adder unit cell.

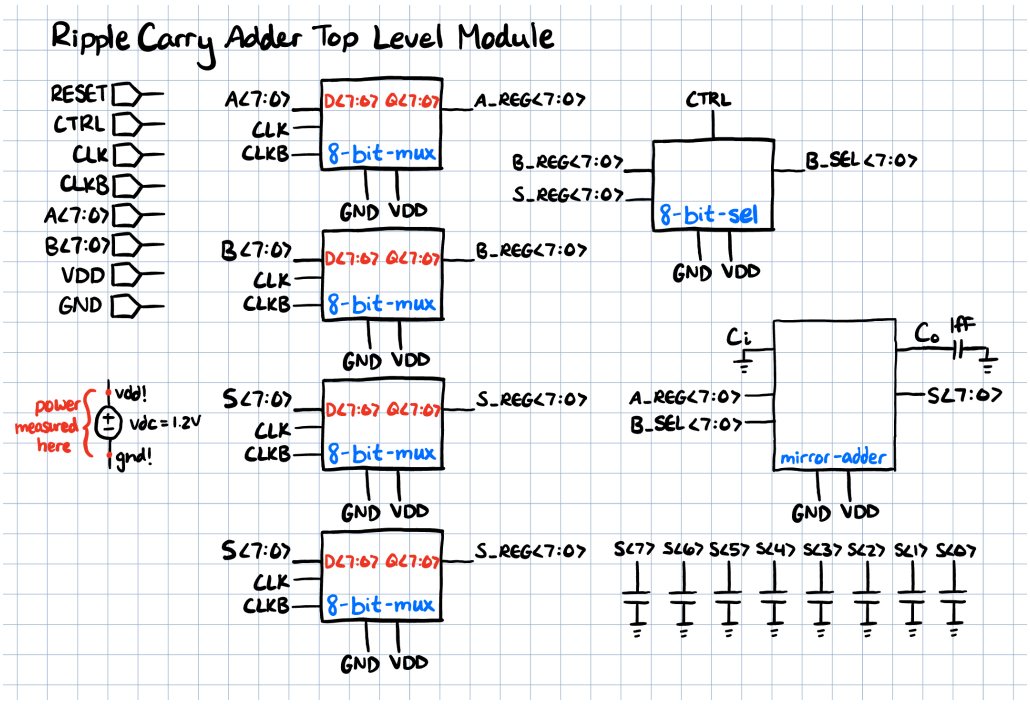

Figure 4: Top-level architectural diagram of the 8-bit dual-mode accumulator.

9.2 Simulation Data and Verification Waveforms

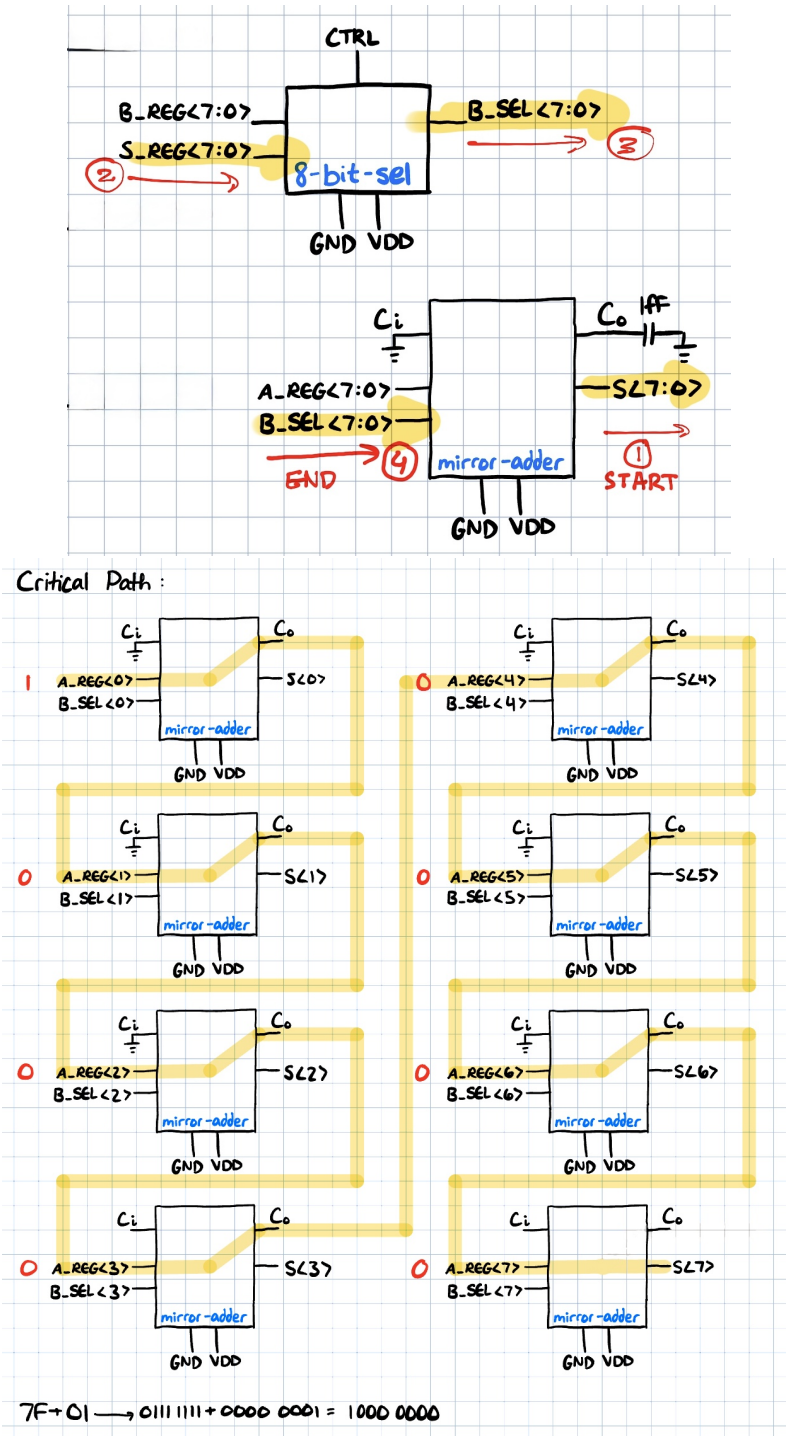

Figure 5: Worst-case critical path visualization for the $01_{16} + 7F_{16}$ pattern.

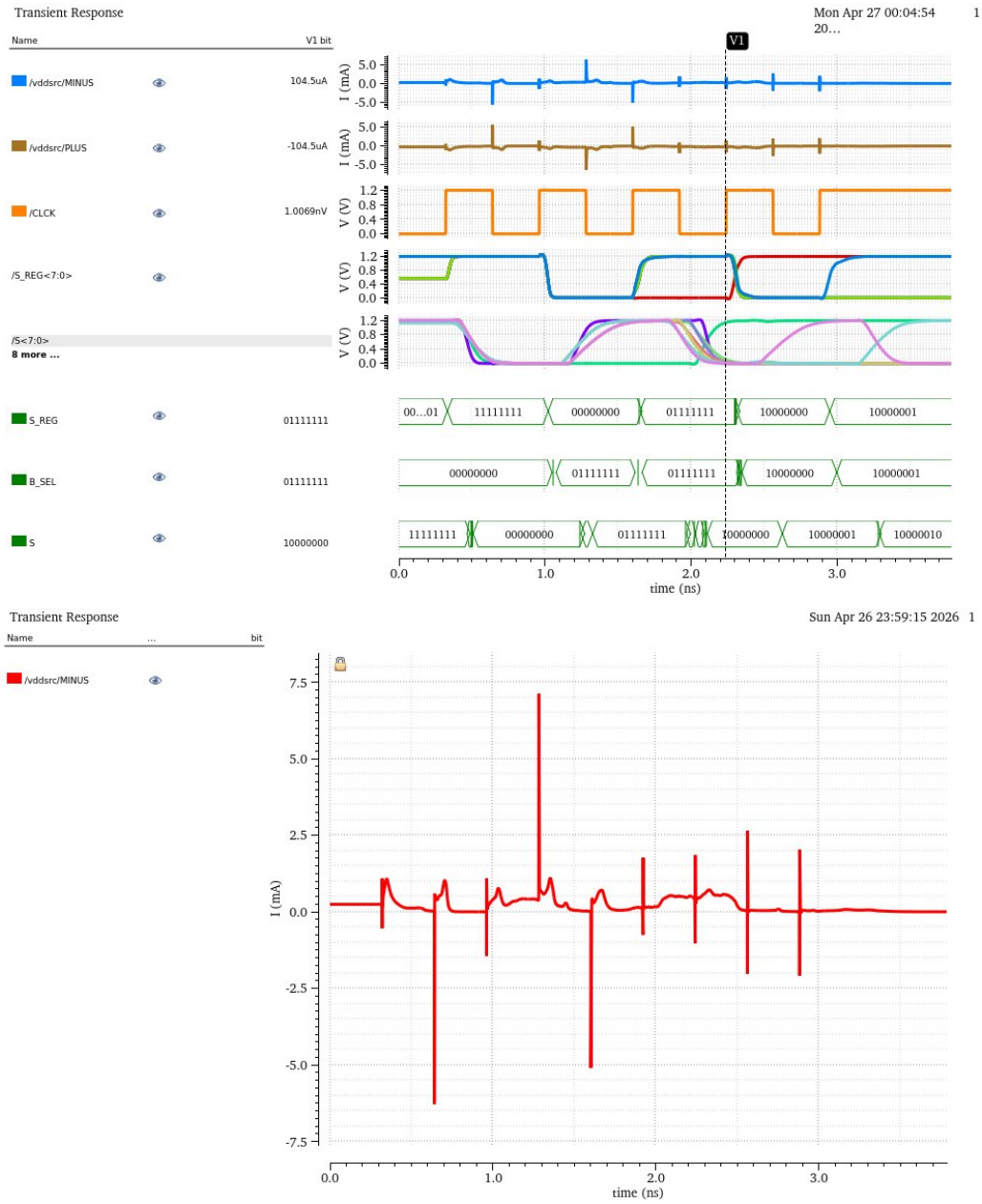

Figure 6: Critical path waveforms for the 1.56 GHz (640 ps) design point.